CORRECTED VERSION

(19) World Intellectual Property Organization

International Bureau





(43) International Publication Date 29 September 2005 (29.09.2005)

PCT

(10) International Publication Number $WO\ 2005/091370\ A1$

(51) International Patent Classification⁷: 21/02, 21/336, 29/786

H01L 27/12,

English

(21) International Application Number:

PCT/JP2005/005064

- (22) International Filing Date: 15 March 2005 (15.03.2005)
- (25) Filing Language:
- (26) Publication Language: English
- (30) Priority Data:

2004-083664 22 March 2004 (22.03.2004) JP

- (71) Applicant (for all designated States except US): SEMI-CONDUCTOR ENERGY LABORATORY CO., LTD. [JP/JP]; 398, Hase, Atsugi-shi, Kanagawa 2430036 (JP).
- (72) Inventors; and
- (75) Inventors/Applicants (for US only): TSURUME, Takuya [JP/JP]; c/o SEMICONDUCTOR ENERGY LABORATORY CO., LTD., 398, Hase, Atsugi-shi, Kanagawa, 2430036 (JP). MARUYAMA, Junya [JP/JP]; c/o SEMICONDUCTOR ENERGY LABORATORY CO., LTD., 398, Hase, Atsugi-shi, Kanagawa, 2430036 (JP). DOZEN, Yoshitaka [JP/JP]; c/o SEMICONDUCTOR ENERGY LABORATORY CO., LTD., 398, Hase, Atsugi-shi, Kanagawa, 2430036 (JP).

- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

- with international search report
- (48) Date of publication of this corrected version:

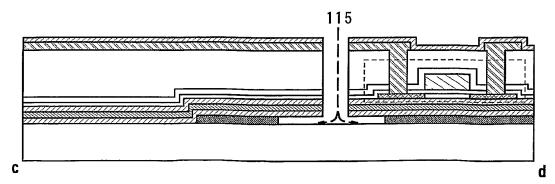
24 November 2005

(15) Information about Correction:

see PCT Gazette No. 47/2005 of 24 November 2005, Section II

[Continued on next page]

(54) Title: METHOD FOR MANUFACTURING INTEGRATED CIRCUIT



(57) Abstract: A method for separating an integrated circuit formed by a thin film having a novel structure or a method for transferring the integrated circuit to another substrate, that is, so-called transposing method, has not been proposed. According to the present invention, in the case that an integrated circuit having a thin film having a novel structure formed over a substrate via a release layer is separated, the release layer is removed in the state that the thin film integrated circuit is fixated, the thin film integrated circuit is transposed to a supporting substrate having an adhesion surface, and the thin film integrated circuit is transposed to another substrate having an adhesion surface with higher strength of adhesion than that of the supporting substrate.

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.